REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-17 are currently pending, with Claims 1-11 withdrawn as directed to non-elected inventions. Claims 12 and 15 have been amended by the present amendment. The changes to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claims 12-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,744,091 to Ema et al. (hereinafter "the '091 patent") in view of U.S. Patent No. 6,433,381 to Mizutani et al. (hereinafter "the '381 patent ").

Claim 12 is directed to a semiconductor device comprising a data holding portion and a peripheral circuit portion that operates in association with the data holding portion, the data holding portion and the peripheral circuit portion being formed on a same semiconductor substrate, the semiconductor device comprising: (1) gate interconnections provided respectively in the data holding portion and the peripheral circuit portion on the semiconductor substrate; (2) first sidewall nitride films provided respectively on sides of the gate interconnections and the data holding portion and the peripheral circuit portions; (3) first and second impurity regions provided in the data holding portion and the peripheral circuit portion, the respective first and second impurity regions being selectively formed in a surface of the semiconductor substrate that extends outward from sides of the respective gate interconnections; (4) sidewall insulating films provided on sides of the first sidewall nitride films of the gate interconnection in the peripheral circuit portion; (5) contact plugs composed of a conductive silicon and passing a first interlayer insulating film provided on the data holding portion to reach the surface of the semiconductor substrate where the first and second

impurity regions are formed; (6) third impurity regions provided in the peripheral circuit portion, the third impurity regions being selectively formed in the surface of the semiconductor substrate that extends outward from the sides of the sidewall insulating film, the third impurity regions having a higher impurity concentration than the first and second impurity regions; and (7) metal silicide films provided on all of the contact plugs in the data holding portion and on the surface of the semiconductor substrate in the peripheral circuit portion where the third impurity regions are formed. Claim 12 has been amended for the purpose of clarification only and no new matter has been added.

Regarding the rejection of Claim 12 under 35 U.S.C. § 103, the Office Action asserts that the '091 patent discloses everything in Claim 12 with the exception of the third impurity regions, and relies on the '381 patent to remedy that deficiency.

The '091 patent is directed to a semiconductor storage device with a self-aligned opening and a method of manufacturing the semiconductor storage device. As shown in Figure 1, the '091 patent discloses a semiconductor storage device that includes a memory cell region and a peripheral circuit region. However, as admitted in the Office Action, the '091 patent fails to disclose third impurity regions provided in the peripheral circuit region, as recited in Claim 12. Moreover, Applicants respectfully submit that the '091 patent fails to disclose sidewall insulating films provided on sides of the first sidewall nitride films of the gate interconnection in the peripheral circuit portion. Rather, the '091 patent merely discloses sidewall nitride films provided on the sides of a gate electrode. Further, Applicants respectfully submit that the '091 patent fails to disclose metal silicide films provided on the surface of the semiconductor substrate in the peripheral circuit portion where the third impurity regions are formed. Since the '091 patent fails to disclose the third impurity regions, it must also fail to disclose the metal silicide films provided on the surface of the

semiconductor substrate in the peripheral circuit portion where the third impurity regions are formed.

The '381 patent is directed to a semiconductor device having a COB type DRAM and a method of manufacturing the same. However, Applicants respectfully submit that the '381 patent fails to disclose (1) third impurity regions provided in the peripheral circuit portion, the third impurity regions being selectively formed in a surface of the semiconductor substrate that extends outward from sides of the sidewall insulating films, the third impurity regions having a higher impurity concentration than the first and second impurity regions; (2) sidewall insulating films provided on sides of the first sidewall nitride films of the gate interconnection in the peripheral circuit portion; and (3) metal silicide films provided on the surface of the semiconductor substrate and the periphery circuit portion where the third impurity regions are formed. In particular, Applicants note that the Office Action refers to col. 24, lines 57-62, in the '381 patent as disclosing the claimed third impurity regions. That section of the '381 patent refers to Claims 1 and 2 of the '381 patent. In particular, Claim 2 of the '381 patent, which depends from Claim 1, recites a "third impurity diffusion layer" in the semiconductor substrate in a peripheral circuit region. However, Applicants respectfully submit that the use of the word "third" in Claim 2 is to distinguish from the claimed "first impurity diffusion layer" and "the second impurity diffusion layer" recited in Claim 1. Moreover, the first paragraph of Claim 1 makes clear that the first and second impurity diffusion layers are formed in the memory cell region, not the peripheral circuit region. Thus, the '381 patent fails to disclose a peripheral circuit portion having first, second, and third impurity regions, as recited in Claim 12. Further, Applicants respectfully submit that the '381 patent fails to disclose that the third impurity region is formed in a surface of the semiconductor substrate that extends outward from sides of the sidewall insulating films, or

that the third impurity regions having a higher impurity concentration than the first and second impurity regions, as recited in Claim 12.

Thus, no matter how the teachings of the '091 and '381 patents are combined, the combination does not teach or suggest the (1) sidewall insulating films; (2) third impurity regions; and (3) the metal silicide films provided on the surface of the semiconductor substrate in the peripheral circuit portion where the third impurity regions are formed, as recited in Claim 12. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of Claim 12 (and dependent Claims 13 and 14) should be withdrawn.

Claim 15 recites limitations analogous to the limitations recited in Claim 12. Accordingly, for the reasons stated above for the patentability of Claim 12, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of Claim 15 (and dependent Claims 16 and 17) should be withdrawn.

Thus, it is respectfully submitted that independent Claims 12 and 15 (and all associated dependent claims) patentably define over any proper combination of the '091 and '381 patents.

Consequently, in view of the present amendment and in light of the above discussion, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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